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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,429	03/30/2004	Michael A. Faulkner	EMC-04-008	3352

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EXAMINER	
BAUER, SCOTT ALLEN	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 02/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/812,429	FAULKNER ET AL.	
	Examiner	Art Unit	
	Scott Bauer	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-10,12-17 and 19-23* is/are rejected.

7)☒ Claim(s) *6,11 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/24/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 13, 22 & 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Kates et al. (US 6,137,267).

3. With regard to Claims 1 & 13, Kates et al., in Figure 5, discloses a power supply system comprising: a power supply (V_{DC}); a load (V_O) coupled to the power supply via a power supply line to receive a voltage therefrom; a circuit protection device (500) comprising: at least one switch device (Q1) coupled between the power supply and the load on the power supply line; a first controller (100) coupled to the at least one switch for: monitoring current flow through the at least one switch; maintaining the at least one switch in an ON state while current flows through the at least one switch in a first direction; and causing the at least one switch to toggle to an OFF state if current flowing through the at least one switch (Q1) flows in a second direction (column 5 lines 66-67 & column 6 lines 1-21); and a second controller (502) coupled to the power supply line between the power supply (V_{DC}) and the at least one switch (Q1) and coupled to the at least one switch for sensing an amount of current flowing between the power supply

and the at least one switch and causing the at least one switch to toggle to the OFF state when the current sensed by the second controller exceeds a reference value (column 8 lines 7-38).

4. With regard to Claim 22, Kates et al. discloses a method of providing fault protection in a power supply system, the method comprising: monitoring a current flowing from a power supply to a load via a power supply line; toggling a switch device coupled between the power supply and the load in the power supply line from an ON state to an OFF state when the current begins to flow from the load to the power supply; monitoring the amplitude of the current flowing in the power supply line; and toggling the switch device from the ON state to the OFF state when the amplitude of the current in the power supply line exceeds a reference value. (column 5, lines 40-67 & column 6 lines 1-21).

5. With regard to Claim 23, Kates et al. discloses a fault protection system, comprising: means for monitoring a current flowing from a power supply to a load via a power supply line; means for toggling a switch device coupled between the power supply and the load in the power supply line from an ON state to an OFF state when the current begins to flow from the load to the power supply; means for monitoring the amplitude of the current flowing in the power supply line; and means for toggling the switch device from the ON state to the OFF state when the amplitude of the current in

the power supply line exceeds a reference value. (column 5, lines 40-67 & column 6 lines 1-21).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2-5, 8-10, 14-17, 20 & 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kates et al. as applied to claim 1 above, and further in view of Maxim Data Sheet 19-2735; Rev 0; 1/03 referred to herein as Maxim.

8. With regard to Claims 2, 3, 8, 14, 15 & 20, Kates et al. teaches the power supply system of Claims 1 & 13 wherein, when the output is in a first state, the MOSFET is in the ON state and when the output is in a second state, the MOSFET is in the OFF state.

Kates et al. does not teach that the least one switch comprises a pair of MOSFETS, or that the first controller comprises a first input coupled to the power supply line between the pair of MOSFETS and the power supply, a second input coupled to the power supply line between the pair of MOSFETS and the load, and an output coupled to gate terminals of the pair of MOSFETS.

Maxim, in Figure 3, teaches an ORing MOSFET controller with fastest fault isolation for redundant power supplies. The controller comprises a switch, which is a pair of MOSFETS (Q1 & Q2). Maxim further teaches that the first controller comprises a first input (V_{CC}) coupled to the power supply line between the pair of MOSFETS and the power supply (OUT_+), a second input coupled to the power supply line between the pair of MOSFETS (CS) and the load, and an output (GATE) coupled to gate terminals of the pair of MOSFETS.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kates et al. with Maxim, by replacing the regulator (100) and battery circuitry (400), taught by Kates et al., with the Oring MOSFET controller taught by Maxim, for the purpose of reducing the size and cost of the protection circuitry by integrating all the circuitry taught by Kates et al. into a single inexpensive (Maxim, General Description lines 3-6) package which is 2.95 mm by 3.05 mm. In the circuit taught by Kates et al., the line current is sensed by a resistor (R1) and an amplifier sends a voltage proportional to the current, to a comparator (526). The reference taught by Kates et al. (520) is replaced by a constant voltage reference (144) as taught by Kates et al in Figure 1, as the controller 504 is removed. The output of 526 is then used as the $\overline{ENABLE}$ signal of Figure 3 taught by Maxim. The switch can be either the signal FET as taught by Kates et al., or the pair of MOSFETS taught by Maxim.

9. With regard to Claims 4, 9, 16 & 21, Kates et al. in view of Maxim discloses the power supply system of Claims 3, 8, 15 & 20. Kates et al further discloses that the second controller comprises a current sensing device (R1) coupled to the power supply line between the power supply and the pair of MOSFETS (Q1 & Q2) for sensing the current in the power supply line and outputting a sensed voltage corresponding to the sensed current, a comparing device (526) for comparing the sensed voltage to a reference voltage (REF) and outputting a first output when the sensed voltage exceeds the reference voltage and a switch (TIMER FET Maxim Fig. 3) coupled between the comparing device and the gate terminals of the pair of MOSFETS, wherein the switch, upon receiving the first output of the comparing device, operates to toggle the pair of MOSFETS to the OFF state. The FET switch coupled to the timer input is coupled to the gates of the pair of MOSFETS through the Maxim controller.

10. With regard to Claim 5, 10 & 17, Kates et al. in view of Maxim discloses the power supply system of Claims 4, 9 & 16. Maxim further discloses that the first controller comprises a timer device (TIMER) and, upon receiving the first output ($\overline{ENABLE}$) from the comparing device, the second controller switch operates to disable the timer device, thus driving the output of the first controller from the first state to the second state, causing the pair of MOSFETS to toggle to the OFF state.

11. Claims 7, 12 & 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kates in view of Maxim as applied to claims 2-5, 8-10, 14-17, 20 & 21 above, and further in view of Suessmilch (US 3,886,932).

12. With regard to Claim 7, 12 & 19 Kates et al. in view of Maxim teaches the power supply system of Claims 4, 9 & 16.

Kates et al. in view of Maxim does not teach that upon receiving the first output from the comparing device, the second controller switch operates to pull the control terminals from the first state to the second state, causing the pair of MOSFETS to toggle to the OFF state.

Suessmilch, in Figure 1, teaches an over current protection circuit wherein the voltage drop across a sense resistor (2) is measured by and evaluation circuit (5) and sent to a comparator (6). Upon receiving an over current output from the comparing device, the controller switch (7) operates to pull the control terminals from a first state to a second state, causing a switch (3) which is a MOSFET, to toggle to the off state (column4 lines 23-37).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kates et al. in view of Maxim with Suessmilch, by coupling the second controller switch taught by Maxim to the gate of the MOSFET pair instead of the timer input, for the purpose of reducing the amount time required for circuit shutdown by bypassing the circuitry of the ORing controller, thus further protecting the load from excess current.

Allowable Subject Matter

13. Claims 6, 11 & 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. Claims 6, 11 & 18 would be allowable if rewritten in independent form including all of the limitations of the base claim because the prior art of record does not teach or fairly suggest a power supply system of Claim 4 comprising an under voltage protection device wherein a second controller switch operates to enable the under voltage protection device, thus driving the output of the first controller from the first state to the second state.

Maxim, in the Figure "UVP FAULT WAVEFORM"", teaches that the gate output switches from a first state to a second state, when the under-voltage protection input drops below a certain voltage level. However, the prior art of record does not teach that the pin can be driven low with a switch when the current sensed by the second controller exceeds a reference value.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Sears (US 4,241,372) teaches a power supply protective circuit wherein the voltage drop across a sense resistor (12) is monitored by a difference amplifier (A). The difference amplifier sends a voltage to a comparator (C) which

compares the voltage to a reference voltage (Ref). When the voltage is higher than the reference voltage, a signal is sent to a controller switch (T_3), which then disconnects the load from the power supply.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Bauer whose telephone number is 571-272-5986. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAB
02/13/2006

PHUONG T. VU
PRIMARY EXAMINER